PORTABLE CONSUMER ELECTRONICS

PACKAGING, MATERIALS, AND RELIABILITY

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Foreword

Anyone who has walked the showroom floor at a recent Consumer Electronics Show (CES) event and taken in the sheer volume and scale of consumer electronic devices available today cannot deny that a revolution has taken place. Faster, cheaper, smaller, sleeker, and more powerful have become buzzwords, and the demand for high-function portable electronic devices continues to grow at a dizzying pace. Where portable devices in the past provided singularly vertical experience, they now provide a dizzying array of integrated scenarios such as reading, browsing, photographing, communicating, viewing, listening, and productivity. The quality and the expectation for high fidelity on all of these device experiences is dramatically different today than five years ago, and will continue to develop exponentially in the coming years. Adding to the complexity of these product categories is the rapidly shrinking product development cycles and product life cycles of most portable consumer electronic devices.

The evolution of electronic packaging has been one of the fundamental driving forces of the explosive growth in portable consumer electronics. The continued evolution to 3-D packaging (die on die and package on package) are examples of the key role packaging evolution has played in the ability to drive smaller and more integrated devices that provide the powerful experiences once only found on desktop and tabletop products. In addition to the technological advance in packaging specific design technology, the corresponding advances in areas such as packaging reliability, materials, assembly technology, and manufacturing test have all come together to make today's portable experiences possible. In the future, new technology areas such as nanotechnology and advances in display technologies will spur the need for further evolutions in packaging and related sciences.

Despite the fact that portable consumer electronic devices constitute one of the fastest growing market segments in the industry, very few

treatises and reference books have been written specifically on this market category. There is a definite need for a source which covers the unique aspects of materials, design, and reliability comprehensively for both the novice who is interested or entering portable electronics field, as well as the practicing engineer who looks to continue to develop in this area. This timely book by Sridhar Canumalla and Puligandla Viswanadham fulfills this growing need. Those who are just now embarking on a career in consumer and portable electronic packaging will benefit immensely from this book. Those of us who are longtime practitioners will find it a relevant reference and compelling read while giving us a glimpse into the future of portable electronic devices.

This book will be a valuable addition to the growing electronic packaging literature, especially as related to portable electronics. Sridhar Canumalla and Puligandla Viswanadham bring to bear more than 50 collective years of academic and industrial experience to this effort. Their combined experience covers a broad spectrum of electronic packaging development including mechanics, materials, failure analysis, chemistry, and reliability at companies such as Nokia, Texas Instruments, Raytheon, Sonoscan, and IBM. Viswanadham is currently an adjunct professor of mechanical engineering at the University of Texas in Arlington and Sridhar is a principal engineer in Microsoft's hardware business. The passion that both of the authors have for this field will be readily apparent to all that read this book.

It is my sincere hope that the electronic packaging industry will benefit from the fruits of their collective experience, expertise, and effort, and I wish the book the success it truly deserves. Oh and one last thing: if you have a sincere interest in portable consumer electronics, in addition to reading this book, take a trip down to CES in Las Vegas; if you have shiny object syndrome, it doesn't get any better.

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Preface

Portable consumer electronic devices and appliances have been experiencing an explosive growth with ever-increasing consumer acceptance, market penetration, and growth in recent years. The demand for cheaper, faster, and better products continues unabated, accompanied by inexorable trends in miniaturization and integration. In several parts of the world, they are already an integral part of our daily lives. Yet, for this class of consumer electronics, it is safe to say that the field is still in its infancy with immense possibilities for new applications, and the future looks very bright. Electronic packaging for these products often has to break current barriers and enter new frontiers on several fronts and is driven by market pressures to manufacture these devices cheaper, smaller, lighter, and with increasing functionality. This book encompasses aspects of material, design, and reliability engineering, high-volume assembly technology, and failure analysis for this exciting and nearly ubiquitous class of consumer electronics.

We write this book to provide a single, comprehensive account of the key aspects of packaging for portable consumer electronic devices including first- and second-level packaging, printed wiring board technology, assembly technology, reliability statistics and engineering, and failure analysis. Aspects of industrial design are considered outside the scope of this book partly because it is more art than science.

We want this book to be useful to practicing engineers, technologists, and designers, and have included several real-life examples of failures and also some discussions of current industry practices. Methods to prevent failures and enhance product reliability are also discussed to reflect our passion for making high quality, reliable, and robust products.

Organization and Scope of Book

This book is written at a level that assumes only a basic knowledge in the fundamentals of physics, chemistry, and engineering at an undergraduate level. The book consists of 10 chapters addressing the various aspects of portable electronics. Adequate cross references are provided at the end of each chapter to enable the uninitiated reader to acquire more detailed information on any given aspect or topic. Since, the focus of the book is portable electronics, a prior understanding of general electronic packaging aspects can be beneficial.

The first chapter introduces and defines the landscape of portable electronic products. Some of the unique aspects of portable electronics are introduced in this chapter and both user and original equipment manufacturer (OEM) perspectives are discussed. In the second chapter, different packaging challenges for achieving higher integration and miniaturization are discussed with particular emphasis on the design, materials, and manufacturing aspects.

Printed wiring boards (PWBs) are the backbone of most current portable electronic products, and different aspects of PWB technology are described next. Both conventional PWB and high-density interconnection technologies are discussed with additional discussion on flexible PWBs. Also, embedded integrated modules are discussed, as they occupy a prominent place on the horizon of PWB landscape.

First-level packaging, namely, packaging the semiconductor device, is common across both portable and non-portable consumer electronic products and is relevant to portable electronic products; hence, it is reviewed in chapter 4. In addition to leaded and leadless packages, area array packages including ball grid array package (BGA), chip scale package (CSP), as well as flip chip and land grid array packages are discussed. Techniques to achieve higher levels of integration using stacked Si and stacked packages, as well as emerging trends are discussed in detail.

Interconnection technologies, the methodologies of attaching two different parts of an electronic assembly, are described in chapter 5. It provides a general overview of the various interconnection schemes that include mechanical, alloy, and adhesive interconnections. While insertion mount technology is discussed only contextually, surface mount technology with different lead and termination configurations is described in some detail with reliability implications. These include leadless chip carriers, quad flat non-leads (QFNs), J-, gull wing, thin small-outline packages (TSOPs), ball grid array (BGA), and chip scale

package (CSP) area array interconnections. Owing to the ROHS and WEEE initiative, tin–lead alloys are being replaced with multicomponent lead (Pb)-free alloys. Tin–silver–copper alloys have been discussed in some detail with their merits and demerits. A discussion of surface finishes and their importance is also included. Adhesive interconnections include isotropic, anisotropic, and intrinsic adhesives and their current status. The chapter concludes with a brief description on optoelectronic connections.

Because the focus of the book is portable electronics where surface mount assembly is the norm, insertion mount or through-hole assembly technology has not been discussed. Even though through-hole assembly is a more robust technology, it is very inefficient in terms of packaging density and hence is not practiced in portable electronics manufacturing. Different aspects of surface mount assembly such as paste printing, component placement, reflow, etc. are described. Rework and repair operations as well as reliability enhancement with underfills are included. A discussion of flexible electronic assemblies is also included in this chapter. This completes the building of the product, and subsequent chapters focus on the reliability and failure analysis of portable electronic products.

The background mathematical concepts for reliability evaluation and engineering are described and discussed in chapter 7. The emphasis is on practical working knowledge, such as techniques to ascertain if there is an improvement in reliability after design changes. General recommendations on interpretation of probability plots for reliability data analysis are also made using several real-life examples. In chapter 8 we discuss the state-of-the-art in reliability engineering of portable consumer electronic products and the environments that are unique to them. A review of the latest practices and trends in assessment of thermo-mechanical, mechanical, and environmental reliability is provided, along with a section devoted to practical considerations in accelerated reliability testing.

Typical failure mechanisms found in portable electronic products and a brief review of analytical techniques commonly employed to understand these failures are presented in the next chapter. Also included are sections on best practices to avoid failures and on a framework for product development to prevent failures.

In the last chapter, we discuss several near-term emerging trends and extrapolate future trends in IC packaging, PWB technology, display technology, energy sources, nanomaterials, wearable electronics, sensor technology, compliant mechanics, self-powered electronics, and

biodegradable electronics. As the technology evolution is extremely rapid, it is thought reasonable to provide a glimpse in to the future, fully recognizing that in very few years these technologies will be the order of the day.

We are grateful to our many of friends and colleagues across the electronic industry in general and our esteemed colleagues at International Business Machines, Motorola, Texas Instruments, Raytheon, Nokia, Sonoscan, and Microsoft in particular. Our association and interactions with them enriched not only our personal lives but also our scientific and technological background. The valuable discussions we had with many of them contributed to a better understanding of the complexities and nuances in the emerging technologies.

We thank our families for the constant and enduring support and encouragement throughout the preparation of this book.

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1

Introduction

Few products in the history of mankind with the technological complexity of portable electronics can compare with the mass market penetration achieved by these nearly ubiquitous devices in the last score or so years. The world has gone digital first and subsequently mobile. Indeed, it is no understatement that the field of electronics, especially portable electronics, has revolutionized several aspects of the way we live, work, entertain ourselves, and communicate to such an extent that almost any prediction of the future state is fraught with large uncertainties. For example, in several developing countries phone penetration rates have exploded primarily as a result of people rejecting the traditional land-line phones in favor of an en masse adoption of mobile phones with concomitant precipitous drops in the cost of connecting individuals. The market disruptions due to portable electronics have been unprecedented and have occurred faster than anticipated. For example, within approximately 10 years, the business model of pay phones at public places has been all but abandoned in direct homage to the exploding mobile phone usage. The manufacturing of consumer electronics is by far the largest and fastest growing industry in the world. It is not surprising that it surpasses many of the traditionally large industries, such as automotive, within a very short time since inception.

Indeed, it is fair to say that mankind has been having an increasingly torrid love affair with portable electronic products, and we carry a multitude of these devices on our person. A businessman might carry a personal digital assistant (PDA), a mobile phone, a laptop computer, an electronic translator, a portable projector, digital music player, portable gaming device, a Bluetooth technology headset, etc. We are also increasingly using electronics in cars, inside homes, in the classroom, and in work places. It is instructive to examine the context of the term "portable electronics."

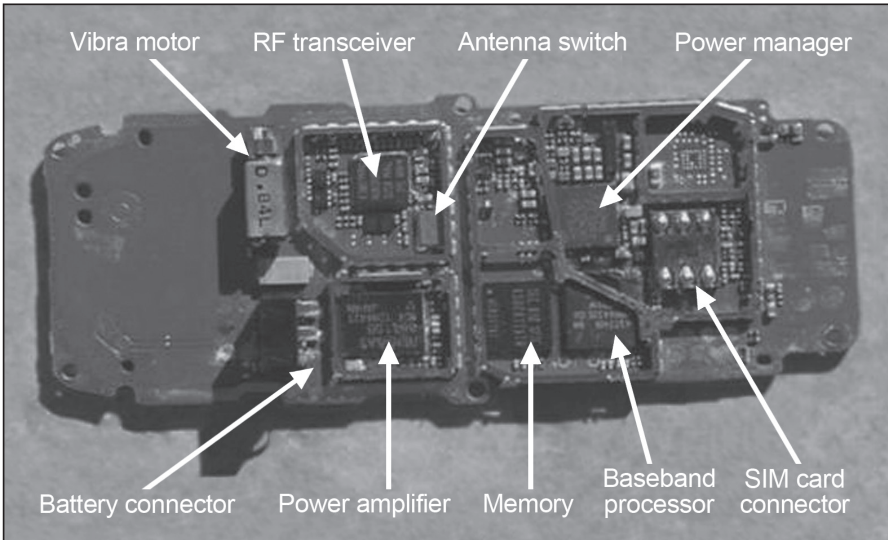

Fig. 1–3. Main printed wiring board (PWB) of an entry-level phone with major components identified

Key Attributes of Portable Electronics—A User's Perspective

Some attributes of portable electronics from a user's perspective can be listed as follows (not in the order of importance):

1. **User friendly.** Key attributes of portable electronics include the size and weight because bulky or heavy devices are not convenient for use by people on the move. In addition, most users gravitate to an ergonomic user interface, and this includes both hardware and software aspects of the product. For example, the scroll wheel commonly found in most e-mail devices or versions of the click-wheel found on most portable music players are user-interface variants that have survived natural selection in the evolutionary battle of the marketplace where only the fittest survive. Long battery life or usage times are also highly prized by users who have to operate far away from recharging stations, sometimes for several days at a time. Ubiquitous usage capability also sets apart the best of the breed from the rest of the pack, and this includes the ability to see the display under a variety of lighting conditions as well as surviving humid conditions,

1. Materials
    a) Cu = 2.7–3.5 oz./gal
    b) Pyrophosphate = 19.4–26.3 oz./gal
    c) Orthophosphate = 8 oz./gal
    d) Ammonia = 0.2–0.3 oz./gal
    e) PY61 = 0.25 0 0.75 ml/A.h (PY61 additive is dimercaptothiadiazole)
2. Process condtions:
    a) pH = 8.1–8.5
    b) Temperature = 111–125°F
    c) Cathode current density = 20–35 A/ft^2

The overall plating process is a reduction of Cu^{2+} ions to metallic copper at the cathode as shown in the following reaction:

$$Cu^{2+} + 2e = Cu\ (s) \tag{3–9}$$

Pulse plating

Sometimes, in plating thick PWBs with high-aspect-ratio through-holes and fine line features, some amount of mushrooming occurs in conventional direct current plating. This limits the closeness of the features due to concerns of shorting and spacing violation. This is overcome using pulse plating with higher than conventional current densities.

In conventional plating, the anodes are covered with an unknown layer that is only slightly soluble in the acid medium. This unknown layer blocks the current, thus passivating or polarizing the anode. By reversing the polarity of the current, the PWB is made the anode for a very brief interval. During the forward pulse, copper is deposited on the entire PWB surface. In the case of through-holes, more copper is plated at the entrance and exit of the hole while the hole interiors have relatively thinner plating. The plating assumes a dog-bone shape. When the polarity is reversed, the PWB becomes the anode and the additive is attracted to the edges of the entry and exit areas of the holes, which also assume a dog-bone shape. When the pulse is reversed, the areas not shielded by the additive get plated with copper and the barrier is dissolved in the process during the first part of the forward plating. Copper deposition continues during the second part of the forward plating step. The last half of the forward pulse completes the dog-bone

such as pH, temperature, time, etc.; (2) inadequate rinsing that can leave residues of grain modifiers, brightners, and other additives on the plated surface; (3) heavy-element contamination; (4) accumulation of decomposition products of the bath when the plating baths are idling at the operating temperature; and (5) variations in bath loading.

In the past, the interconnection pad sizes were relatively large, as the industry was not practicing fine-pitch high-density package assembly. Thicker and less porous gold surface was acceptable. More aggressive organic solvents or water cleanable fluxes were in use. Pad to defect ratio was large and hence there was still enough good pad area to provide an acceptable interconnection. On the other hand, with the advent of fine-pitch surface-mount technology and the introduction of 0.5 and 0.4 mm pitch chip-scale packages, the feature sizes and pad sizes have become smaller and smaller. Use of thicker and less porous gold is a cause of concern in joint embrittlement. Migration to no-clean, less aggressive fluxes made the problem even more obvious. In addition, the pad to defect ratio is much smaller and there is not enough good pad area to give good interconnection. Cost competitiveness may lead to processing more boards through the line and less rigorous process control and monitoring etc. Since the first reporting of this solderability problem, industry has taken several steps to minimize and alleviate the problem through better process control, monitoring, and changes in plating formulations. Still, an occasional appearance of black pad defect cannot be ruled out. Other solutions include migration to electroplating of nickel, two-stage Au plating consisting of immersion and electroless Au, etc.

Typical thicknesses of the common PWB surface finishes are shown in table 3–6.

Table 3–6. Typical thicknesses of the various PWB finishes

Surface Finish	Typical Thickness μ/(μ-inches)
Electroless Ni/electroless Au	3–6 /(120–240) Ni and 0.25–1.3/(10–50) Au
Electroless Ni/immersion Au	2.5–5 /(100–200) and 0.05–0.23 (2–9) Au
Ni//Pd/Au	25 (100–200)Ni/0.2–0.6(8-24)Pd/0.02–0.05(1–2) Au
Immersion Ag	0.15–0.45 (6–8)
Immersion Tin	0.6–1.6 (25–60)
Immersion Pd	0.1–10 (4–400)
Hot air solder level	0.65–50/(25–2000)
Organic solder preservative	0.2–0.6 (8–24)

portable electronic appliances. In majority of cases, leaded packages are limited to gull wing packages. J-leaded packages are rarely used and hence do not constitute an integral part of this chapter. Low profile and high packaging efficiency impose constraints on CTE mismatch and lead compliance and hence have an impact on package-to-board interconnection reliability.

Owing to the form factor definition, space constraints, and high packaging density requirements of portable electronic products, thinner packages of low profile and lead pitch finer than 0.8 mm as well as higher packaging ratio have emerged. The products include personal computer memory card industry association (PCMCIA) cards, personal digital assistants (PDAs), cell phones, camcorders, digital cameras, etc. Thus evolved thin quad flat packs, thin small outline packages (TSOPs), very small shrink outline packages (VSSOPs), etc.

PCMCIA cards are of the size of conventional credit cards except they are thicker (85 mm × 54 mm × 3 mm). Data can be transferred from one computer to another with great ease. These packages enabled versatility, functionality, and flexibility in product design of many portable electronics and the eventual emergence of high-density packaging.

The predetermined form factor, however, imposed severe restrictions on packaging. The multilayer PWB has to be much thinner than the conventional boards (about 0.25–0.5 mm), and the first-level packages need to be of very low profile, especially if the assembly is a double-sided one. The packages are of very low profile, made of thinner silicon, and are finer in lead pitch. The packages have very small outline, implying that the package is not very much larger than the silicon device that is packaged.

TSOPs are mainly used for packaging memory devices and are generally of low I/O (under 100). They are rectangular in shape and are of two kinds: Type I and Type II. Type I TSOPs have leads emanating from the shorter dimension of the packages and are generally 0.5 mm in pitch, while in type II TSOPs the leads emanate from the longer dimension side of the package and are of a coarser pitch of either 32 or 50 mils (Viswanadham et al. 1993). The lead material of many of the earlier versions of these packages was alloy-42, and the lead shape is traditionally of the gull wing type. A typical illustration of TSOP I and TSOP II packages is shown in figure 4–14(a) and (b).

Both cavity-up and cavity-down formats are possible for this package, as shown in figure 4–35(a) and (b). The cavity-down version will have a lower pin count in the range 50–100 for applications such as DRAMs, while the cavity-up configuration has a relatively higher pin counts in the 100–300 range for high-performance microcontrollers and digital signal processors (DSPs).

Owing to the materials' choice and design, the package is very moisture resistant and has demonstrated acceptable reliability.

Rigid interposer packages

CSPs are also designed with a rigid substrate interposer. The rigid interposer can be either of ceramic or organic laminate material. The choice of rigid substrate depends on the functionality of the package required. Multilayer or thick-film ceramic interposer may be required for specific high-wattage, high I/O high functionality devices. Organic laminates generally include such materials as bis-maleimide triazine (BT), high-temperature tetra-functional FR-4, etc., and are generally well suited for moderate to low I/O applications, and compatible with organic PWBs.

Amkor chip array package

This package derives its name from the fact that it is manufactured in an array format. The interposer can be either organic or ceramic. The ceramic version is generally used for disk drive applications. The organic interposer is about 0.34 mm thick. The die thickness is 0.3 mm. The first-level interconnect is by gold wire bond on a bond pad pitch of 90 µm. The copper traces on the laminate are Ni- and Au-plated. It is a near-die-sized package (NDSP) with a lead count in the 28 to 128 range and is available in sizes of either 5 × 5 mm or 11 × 11 mm. The second-level interconnect is either solder ball or a land grid array at a variety of pitches in the 0.5–1.0 mm range in single or double row perimeter arrays. The package is overmolded with a resin and is about 0.7 mm in thickness. Figure 4–36 shows a schematic of the package. The package has a self inductance of 1.4–7.8 nH and an impedance of 170 Ω and is generally used for ASIC, memory, analog, and telecommunication applications. Since it is a plastic package, it is sensitive to moisture and is supplied as a level-3 package. In tests, the package survived without failure in the pressure cooker test at 121°C and 100% R.H. for 500 h; temperature, humidity and bias test at 85°C and 85% R.H. for 1000 hr, and thermal shock test of –55–150°C for 1,000 cycles.